Elektronische Bauelemente

SSG06P15V-C

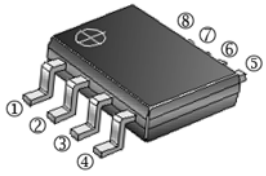
-6A, -150V, $R_{DS(ON)}$ 320mΩ
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

SOP-8

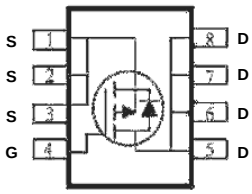


APPLICATIONS

- Brushless motor
- Uninterruptible power supply
- Load Switch

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13 inch



ORDER INFORMATION

Part Number	Type
SSG06P15V-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=-10V [1]	T_A=25℃	I_D	-6	A
	T_A=100℃		-3.2	
Pulsed Drain Current [2]		I_{DM}	-45	A
Power Dissipation [3]		P_D	52	W
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	85	℃/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	1.9	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-150	-	-	V	V_{GS}=0V, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-2	-3	-4	V	V_{DS}=V_{GS}, I_D= -250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{DS}=0V, V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	μA	V_{DS}= -150V, V_{GS}=0V
	T_J=85°C		-	-	-30		
Drain-Source On-Resistance		$R_{DS(ON)}$	-	270	320	mΩ	V_{GS}= -10V, I_D= -3A
			-	300	500		V_{GS}= -6V, I_D= -2A
Gate Resistance		R_G	-	5.4	-	Ω	V_{DS}=V_{GS}=0V, f=1MHz
Total Gate Charge [2 3]		Q_g	-	19.5	-	nC	V_{DS}= -75V V_{GS}= -10V I_D= -2.4A
Gate-Source Charge [2 3]		Q_{gs}	-	4.8	-		
Gate-Drain Charge [2 3]		Q_{gd}	-	5.3	-		
Turn-On Delay Time [2 3]		$T_{d(on)}$	-	8	-	nS	V_{DD}= -75V V_{GS}= -10V I_D= -1.9A R_G=1Ω
Rise Time [2 3]		T_r	-	9	-		
Turn-Off Delay Time [2 3]		$T_{d(off)}$	-	23	-		
Fall Time [2 3]		T_f	-	8	-		
Input Capacitance		C_{iss}	-	880	-	pF	V_{DS}= -75V V_{GS}=0V f=1MHz
Output Capacitance		C_{oss}	-	50	-		
Reverse Transfer Capacitance		C_{rss}	-	35	-		

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed , pulse width≦300μs , duty cycle≦2%
3. The power dissipation is limited by 150℃ juncti on temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

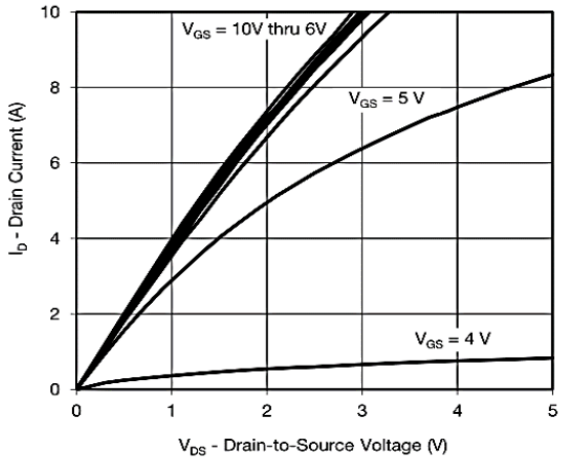


Fig1：Output Characteristics

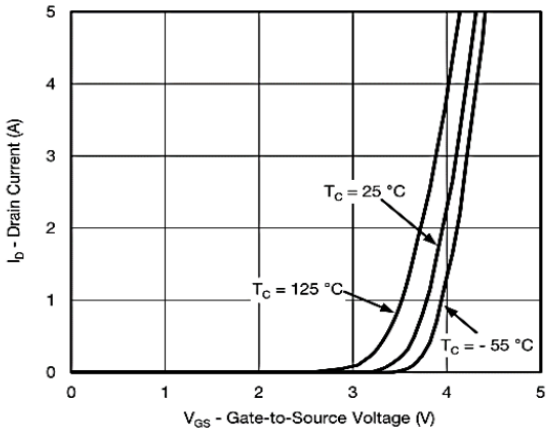


Fig2：Transfer Characteristics

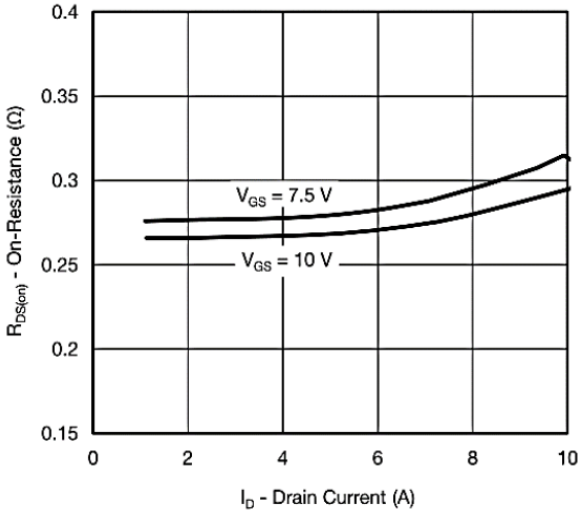


Fig3：On-Resistance vs. Drain Current and Gate Voltage

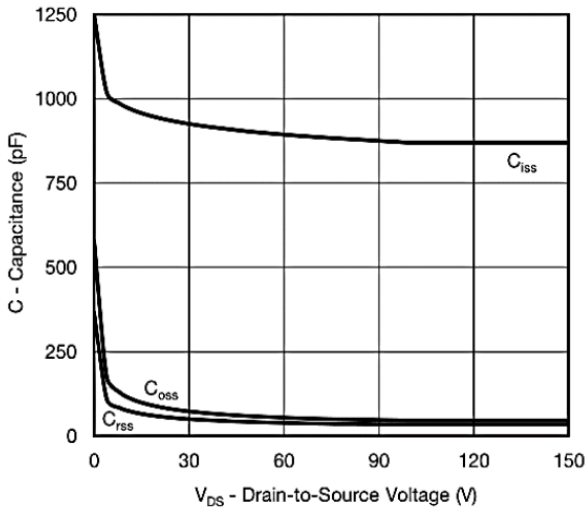


Fig4Capacitance

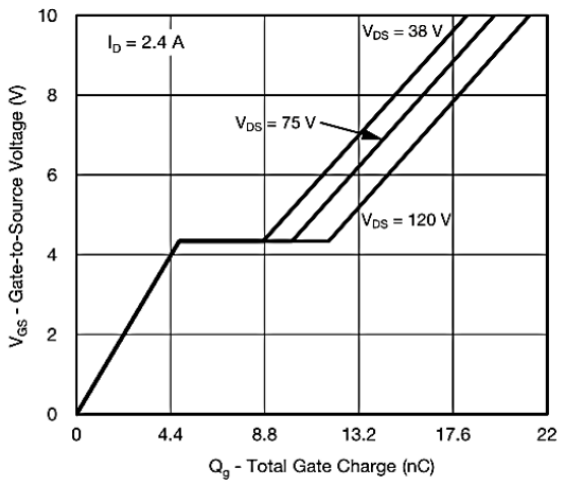


Fig5：Gate Charge

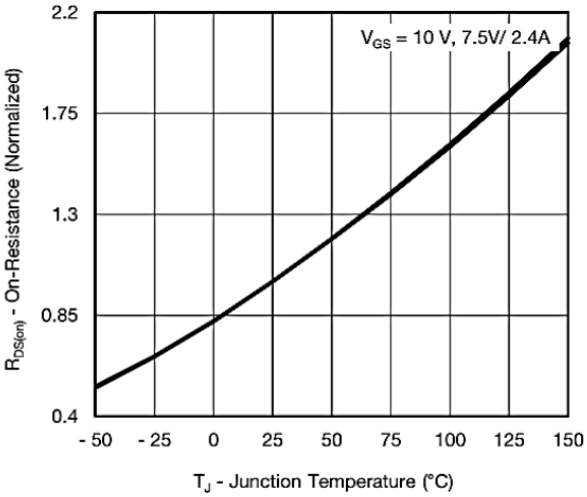


Fig6：On-Resistance vs. Junction Temperature

CHARACTERISTIC CURVES

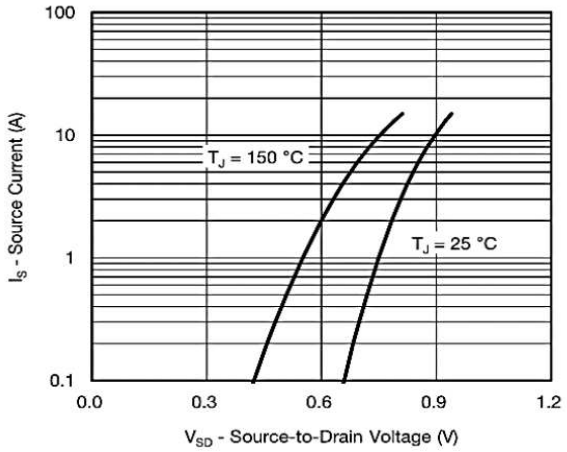


Fig7：Source-Drain Diode Forward Voltage

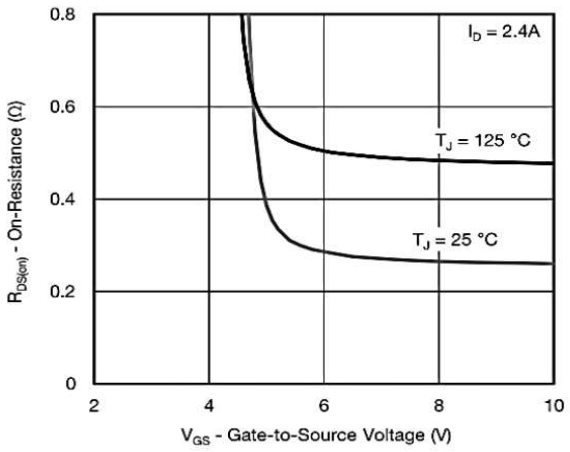


Fig8：On-Resistance vs. Gate-to-Source Voltage

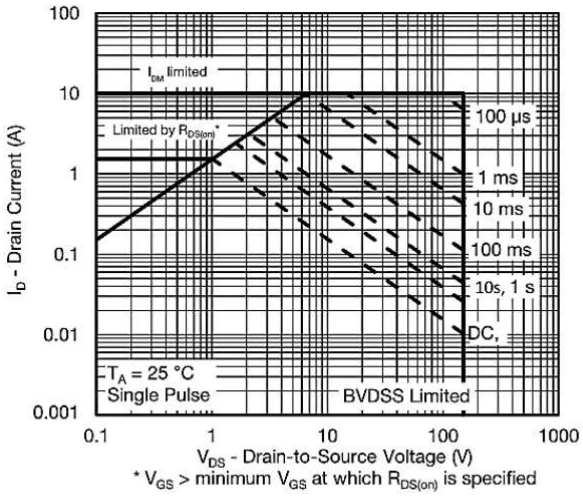


Fig9：Safe Operating Area, Junction-to-Ambient

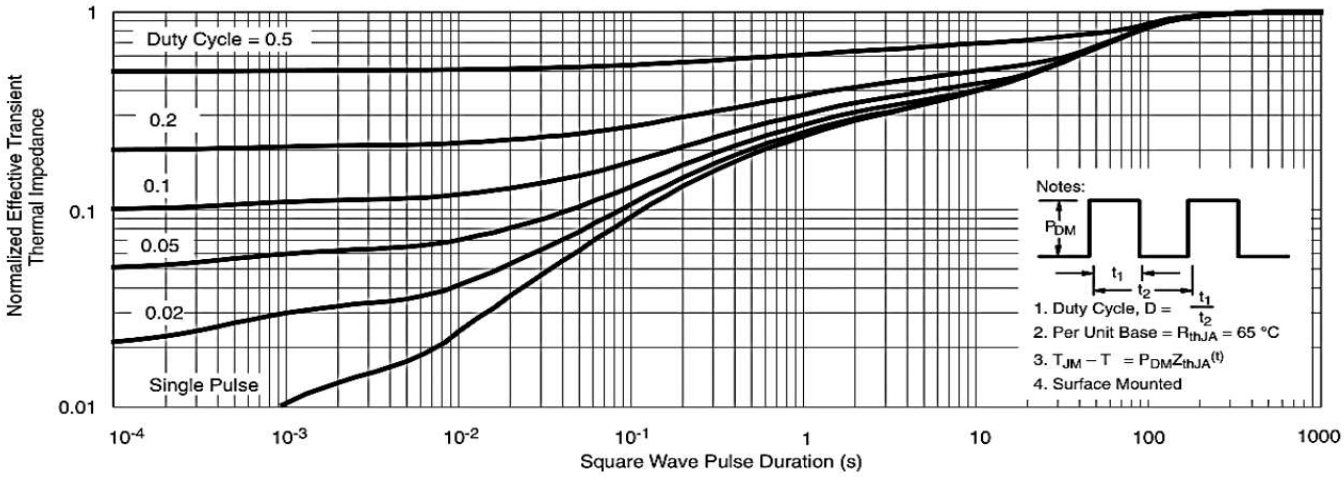


Fig10：Normalized Thermal Transient Impedance, Junction-to-Ambient

PACKAGE OUTLINE DIMENSIONS

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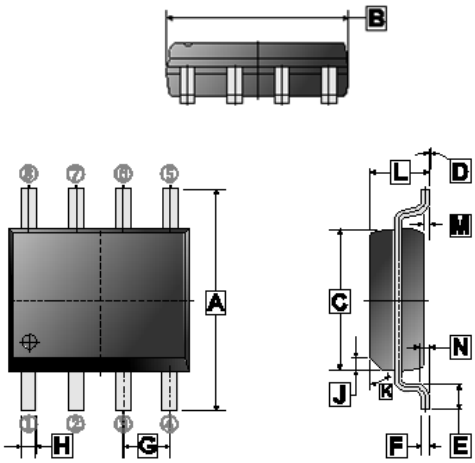

REF.	Millimeter	
	Min.	Max.
A	5.80	6.20
B	4.38	5.20
C	3.70	4.10
D	0°	8°
E	0.40	1.27
F	0.10	0.26
G	1.27 TYP.	
H	0.30	0.51
J	0.375 REF.	
K	45° REF.	
L	1.30	1.80
M	0	0.25
N	0.25 REF.	

MOUNTING PAD LAYOUT

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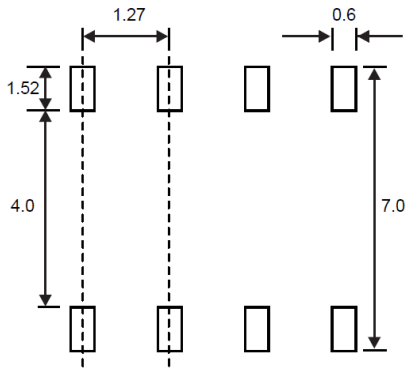

*Dimensions in millimeters