

RoHS Compliant Product
 A suffix of "-C" specifies halogen & lead-free

FEATURES

- Low On-Resistance
- High-Speed Switching
- Drive Circuits Can be Simple
- Parallel Use is Easy

APPLICATIONS

- P-Channel Enhancement Mode Effect Transistor
- Switching Application

MARKING

K84

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOT-363	3K	7 inch

ORDER INFORMATION

Part Number	Type
SUM84DW-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

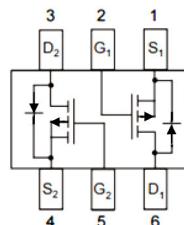
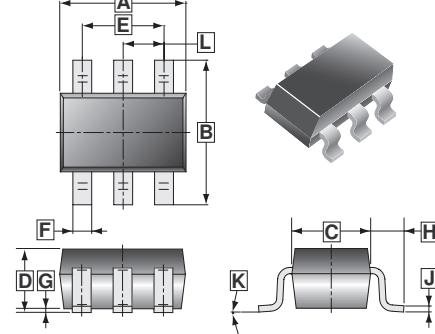
Parameter	Symbol	Ratings		Unit
Drain-Source Voltage	V _{DS}	-50		V
Gate-Source Voltage	V _{GS}	±12		V
Continuous Drain Current ¹	I _D	-0.13		A
Total Power Dissipation ¹	P _D	0.3		W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150		°C
Thermal Data				
Thermal Resistance Junction-Ambient ¹	R _{θJA}	417		°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	-50	-	-	V	V _{GS} =0, I _D = -250μA
Gate Threshold Voltage ²	V _{GS(th)}	-0.8	-	-2	V	V _{DS} =V _{GS} , I _D = -1mA
Gate-Source Leakage Current	I _{GSS}	-	-	±10	nA	V _{GS} = ±12V
Drain-Source Leakage Current	I _{DSS}	-	-	-1	μA	V _{DS} = -50V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	2.1	10	Ω	V _{GS} = -5V, I _D = -0.1A
Turn-on Delay Time	T _{d(on)}	-	6	-	nS	V _{DS} = -30V, V _{GS} = -10V
Turn-off Delay Time	T _{d(off)}	-	25	-		I _D = -0.2A, R _G =25Ω
Input Capacitance	C _{iss}	-	56	-	pF	V _{GS} =0
Output Capacitance	C _{oss}	-	17	-		V _{DS} = -20V
Reverse Transfer Capacitance	C _{rss}	-	5	-		f=1MHz

Notes:

1. Surface Mounted on FR4 Board, t≤10 sec.
2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.80	2.20	G	0.100	REF.
B	1.80	2.45	H	0.525	REF.
C	1.15	1.35	J	0.08	0.25
D	0.80	1.10	K	8°	
E	1.10	1.50	L	0.650 TYP.	
F	0.10	0.35			

CHARACTERISTIC CURVES

FIG 1.OUTPUT CHARACTERISTICS

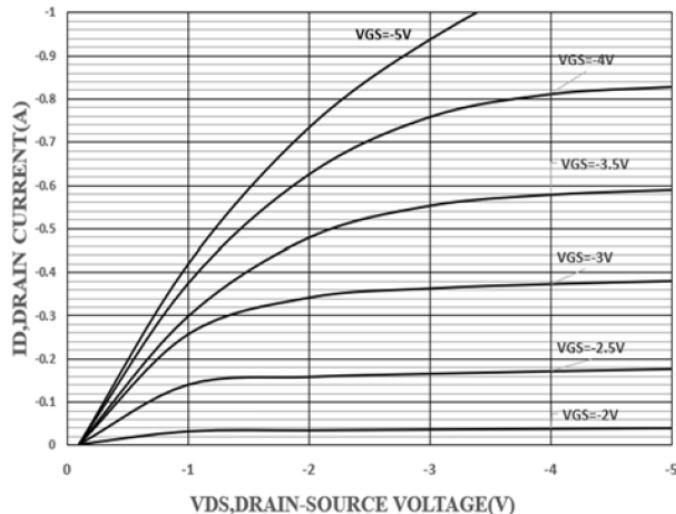


FIG 2.DRAIN-SOURCE ON RESISTANCE

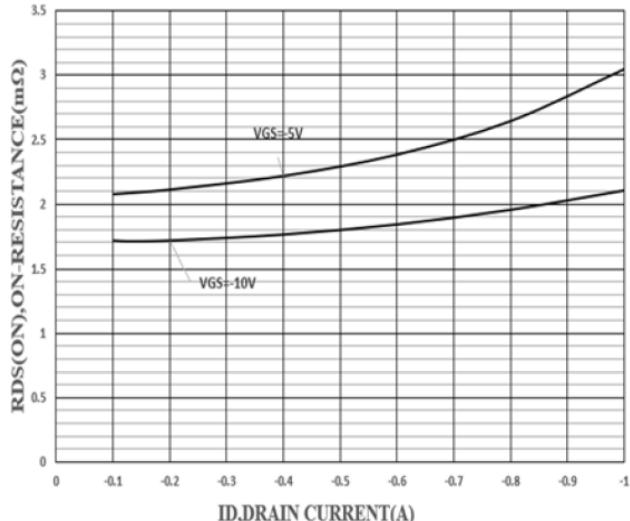


FIG 3.DRAIN-SOURCE ON RESISTANCE

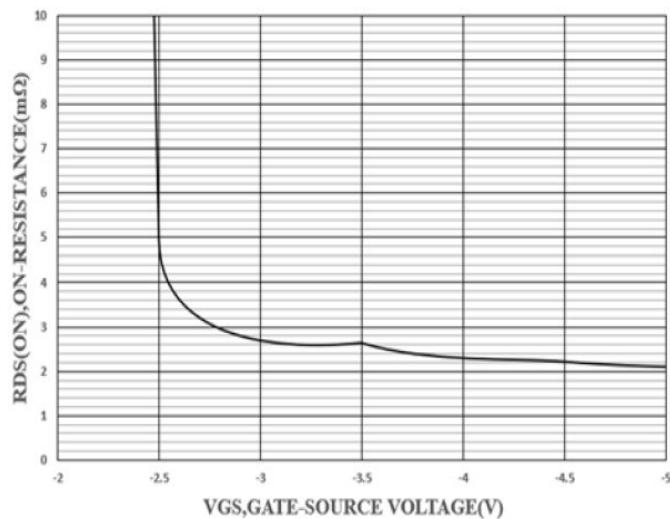


FIG 4.GATE THRESHOLD VOLTAGE

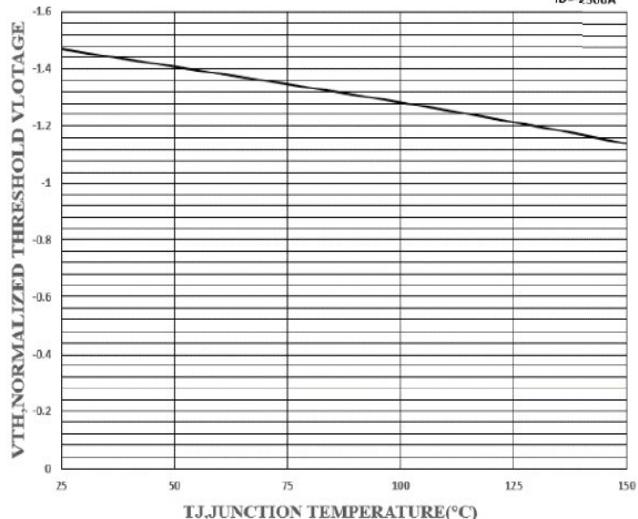


FIG 5.DRAIN-SOURCE ON RESISTANCE

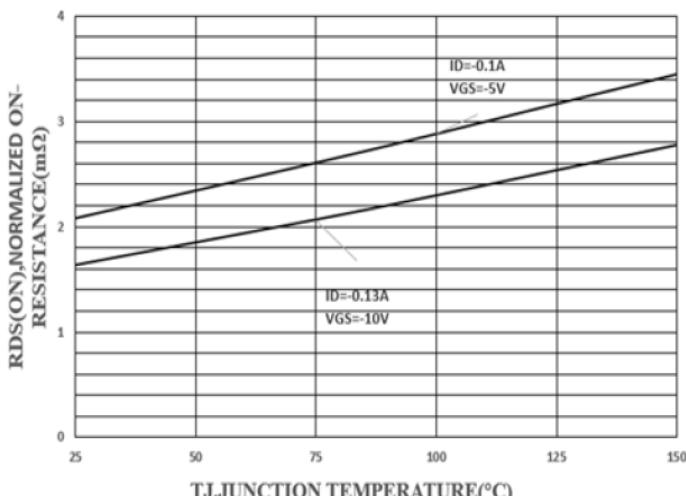


FIG 6.CAPACITANCE

