Elektronische Bauelemente

SSPR100N04S-C

100A, 40V, $R_{DS(ON)}$ 2.7mΩ

N-Channel Shielded Gate Trench Power MOSFET

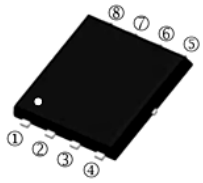
RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSPR100N04S-C is the Shielded Gate Technology N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSPR100N04S-C meet the RoHS and Green Product requirement with full function reliability approved.

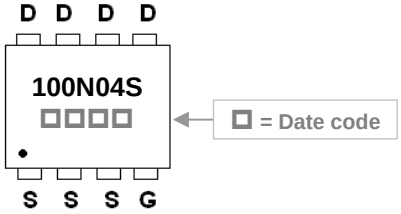
SPR-8PP

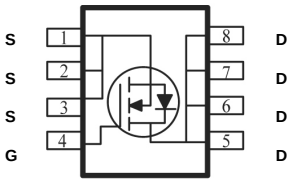


FEATURES

- Shielded Gate Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING





PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR100N04S-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1,5] @V_{GS}=10V	T_C=25℃	I_D	100	A
	T_C=100℃		64	
	T_A=25℃		21	
	T_A=100℃		13.4	
Pulsed Drain Current [2]		I_{DM}	200	A
Power Dissipation [3]	T_C=25℃	P_D	41.7	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	70	℃/W
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	3	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=32V, V_{GS}=0V
	T_J=55℃		-	-	5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	2.2	2.7	mΩ	V_{GS}=10V, I_D=20A
			-	3.3	4		V_{GS}=4.5V, I_D=20A
Gate Resistance		R_g	-	1.7	-	Ω	f=1MHz
Total Gate Charge		Q_g	-	45.8		nC	I_D=20A V_{DS}=20V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	8	-		
Gate-Drain Change		Q_{gd}	-	10.6	-		
Turn-on Delay Time		$T_{d(on)}$	-	15.8	-	nS	V_{DD}=20V I_D=1A V_{GS}=10V R_G=1Ω
Rise Time		T_r	-	9.5	-		
Turn-off Delay Time		$T_{d(off)}$	-	35.6	-		
Fall Time		T_f	-	36.3	-		
Input Capacitance		C_{iss}	-	2643	-	pF	V_{GS}=0V V_{DS}=20V f=1MHz
Output Capacitance		C_{oss}	-	861	-		
Reverse Transfer Capacitance		C_{rss}	-	81	-		
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0V, T_J=25℃
Continuous Source Current [1 4 5]		I_S	-	-	85	A	V_G=V_D=0V, Force Current

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≦ 300us, duty cycle≦ 2%.
3. The power dissipation is limited by 150℃ juncti on temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.
5. Package limitation current is 85A.

CHARACTERISTIC CURVES

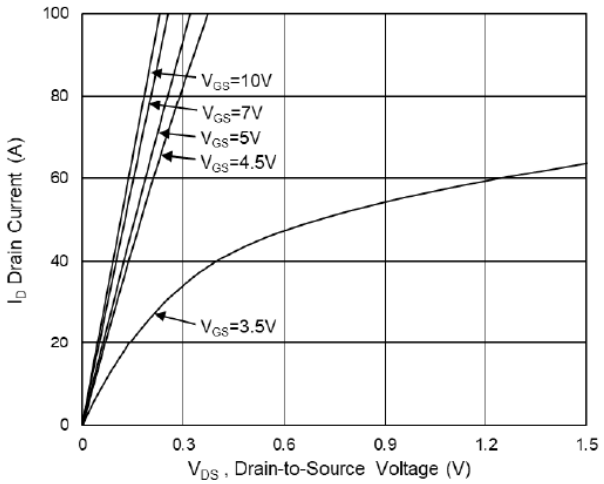


Fig.1 Typical Output Characteristics

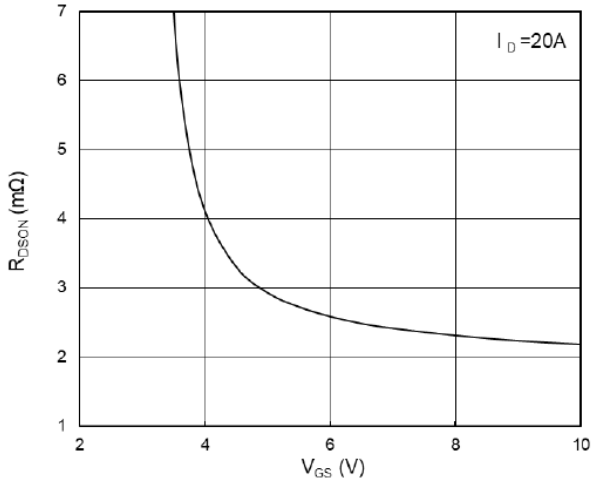


Fig.2 On-Resistance vs G-S Voltage

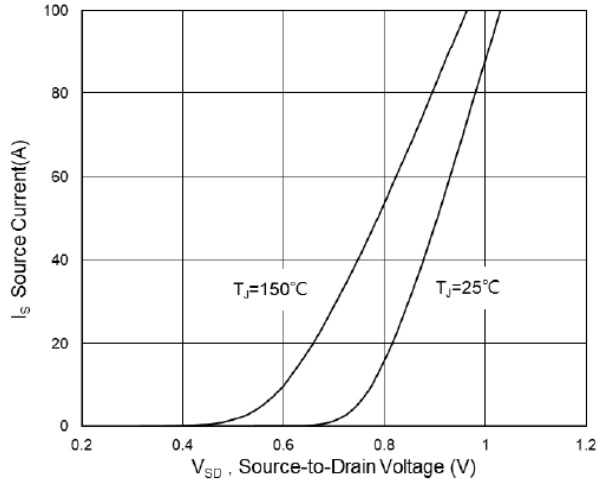


Fig.3 Source Drain Forward Characteristics

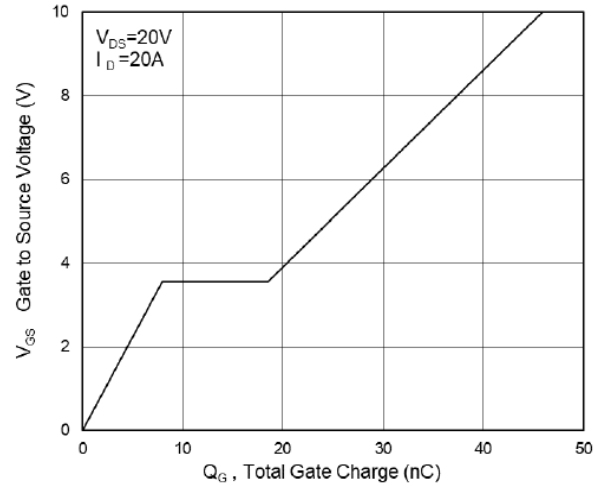


Fig.4 Gate-Charge Characteristics

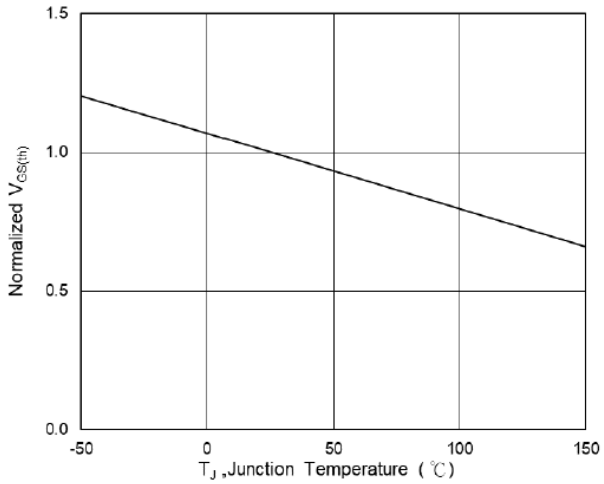


Fig.5 Normalized $V_{GS(th)}$ vs T_J

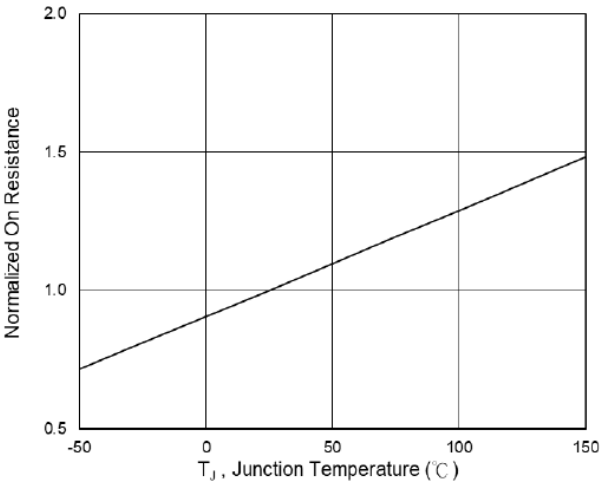


Fig.6 Normalized R_{DSON} vs T_J

CHARACTERISTIC CURVES

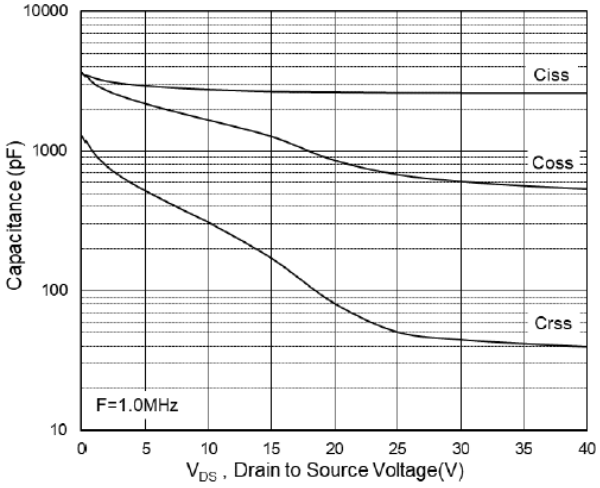


Fig.7 Capacitance

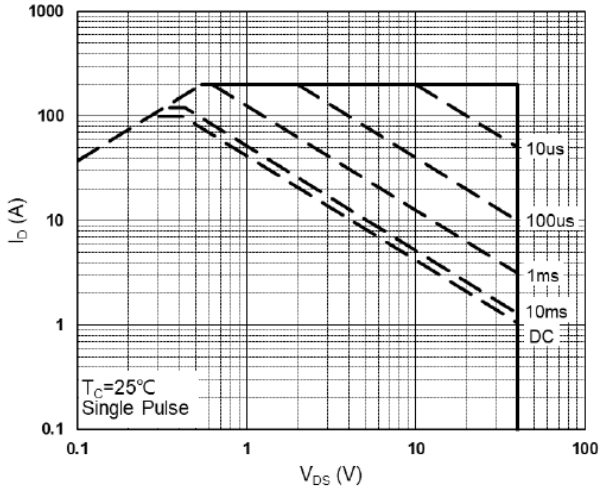


Fig.8 Safe Operating Area

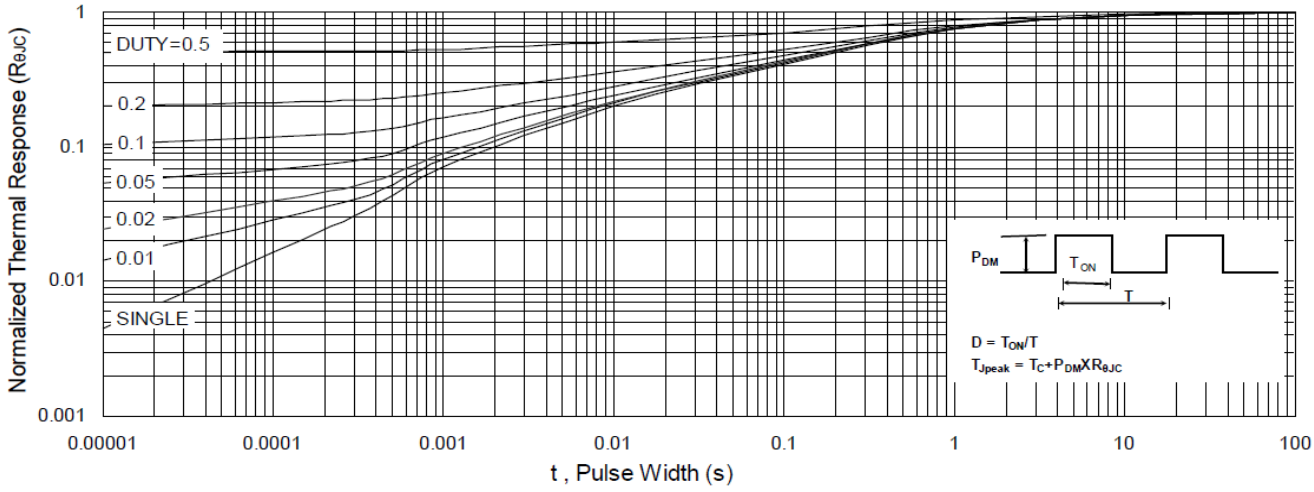


Fig.9 Normalized Maximum Transient Thermal Impedance

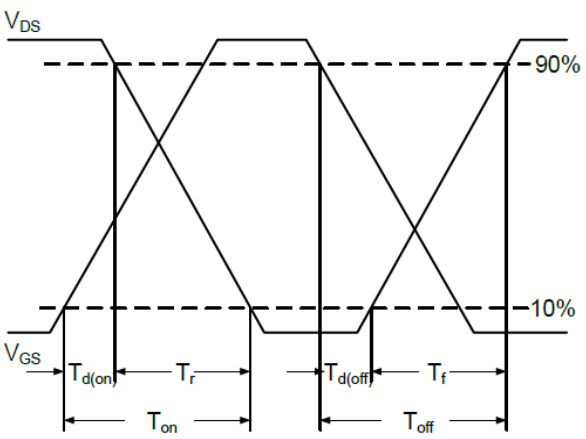


Fig.10 Switching Time Waveform

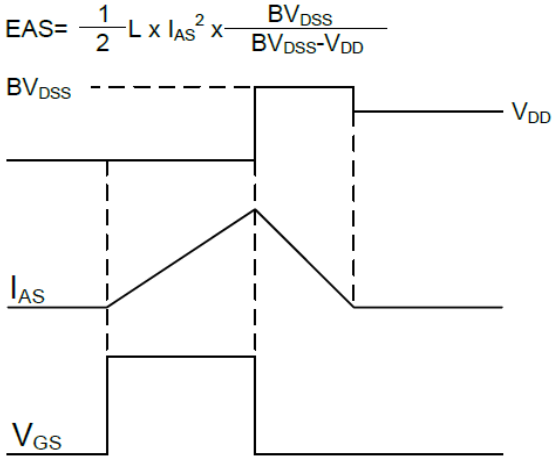
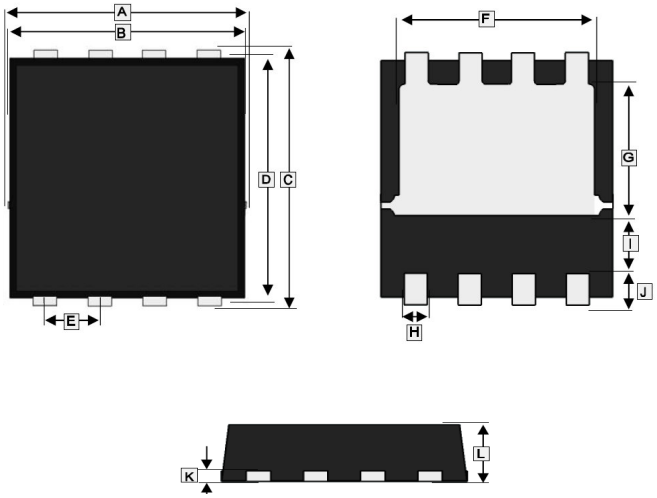


Fig.11 Unclamped Inductive Waveform

PACKAGE OUTLINE DIMENSIONS

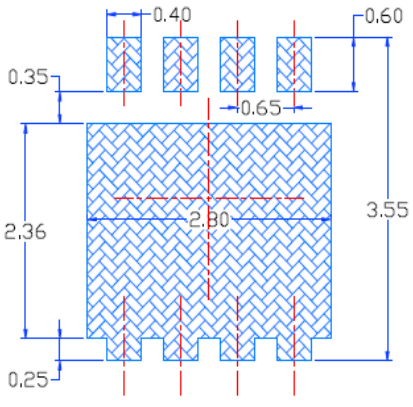
SPR-8PP



REF.	Millimeter	
	Min.	Max.
A	3.00	3.40
B	3.00	3.25
C	3.20	3.45
D	3.00	3.20
E	0.65 BSC.	
F	2.39	2.60
G	1.35	1.98
H	0.24	0.35
I	0.35 TYP.	
J	0.60 TYP.	
K	0.10	0.25
L	0.70	0.90

MOUNTING PAD LAYOUT

SPR-8PP



*Dimensions in millimeters