SSD61N06S-C

61A , 60V , $R_{DS(ON)}$ 9mΩ
N-Ch Enhancement Mode Power MOSFET

Elektronische Bauelemente

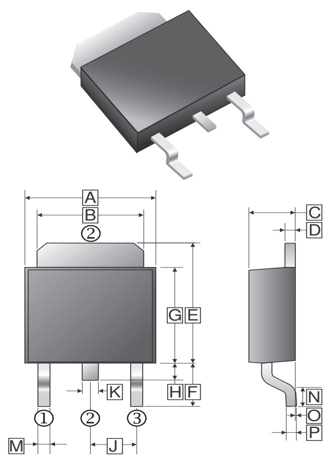
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

SSD61N06S-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provides excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

SSD61N06S-C meets the RoHS and Green Product requirement with full function reliability approved.

TO-252(D-Pack)

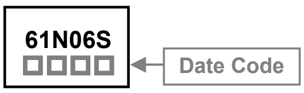


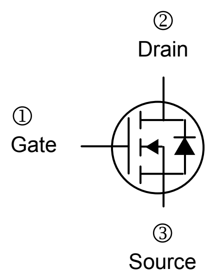
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30 REF.	
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

MARKING





PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD61N06S-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_C=25°C	I_D	61	A
	T_C=100°C		40	
Pulsed Drain Current [2]		I_{DM}	180	A
Power Dissipation	T_C=25°C	P_D	62.5	W
Operating Junction & Storage Temperature		T_J, T_{STG}	-55~150	°C
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	65	°C/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V, V_{DS}=0V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=48V, V_{GS}=0, T_J=25°C
		-	-	100		V_{DS}=48V, V_{GS}=0, T_J=100°C
Static Drain-Source On-Resistance [3]	$R_{DS(ON)}$	-	7.3	9	mΩ	V_{GS}=10V, I_D=20A
		-	10	13		V_{GS}=4.5V, I_D=20A
Transconductance	g_{fs}	-	26	-	S	V_{DS}=5V, I_D=20A
Gate Resistance	R_g	-	1.5	-	Ω	V_{DS}=V_{GS}=0V, f =1MHz
Total Gate Charge (4.5V)	Q_g	-	12	-	nC	I_D=20A V_{DD}=30V V_{GS}=10V
Total Gate Charge		-	24	-		
Gate-Source Charge	Q_{gs}	-	5	-		
Gate-Drain Change	Q_{gd}	-	3	-		
Turn-on Delay Time	$T_{d(on)}$	-	9	-	nS	V_{DD}=30V I_D=20A V_{GS}=10V R_G=10Ω
Rise Time	T_r	-	4	-		
Turn-off Delay Time	$T_{d(off)}$	-	29	-		
Fall Time	T_f	-	4	-		
Input Capacitance	C_{iss}	-	1620	-	pF	V_{GS} =0V V_{DS}=30V f =1MHz
Output Capacitance	C_{oss}	-	415	-		
Reverse Transfer Capacitance	C_{rss}	-	3	-		
Source-Drain Diode						
Diode Forward Voltage [3]	V_{SD}	-	-	1.2	V	I_F=20A, V_{GS}=0V
Reverse Recovery Time	T_{rr}	-	30	-	nS	I_F=20A,V_R=30V,dI/dt=300A/μs
Reverse Recovery Charge	Q_{rr}	-	43	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width ≤300μs, Duty Cycle≤2%
3. The Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

CHARACTERISTIC CURVES

Fig 1. Typical Output Characteristics

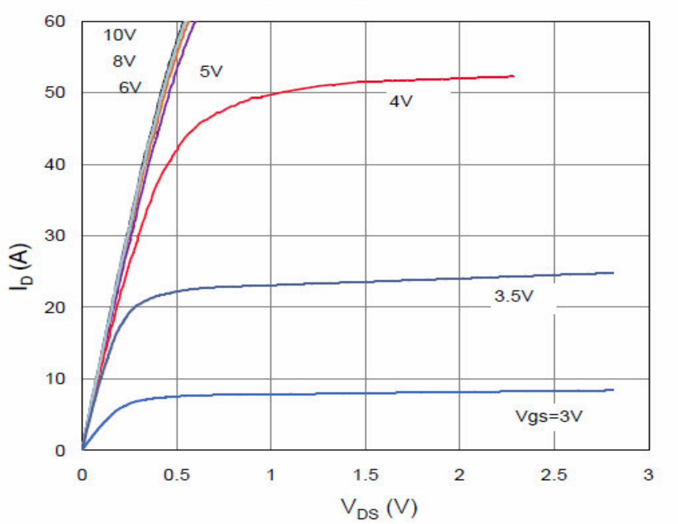


Figure 2. On-Resistance vs. Gate-Source Voltage

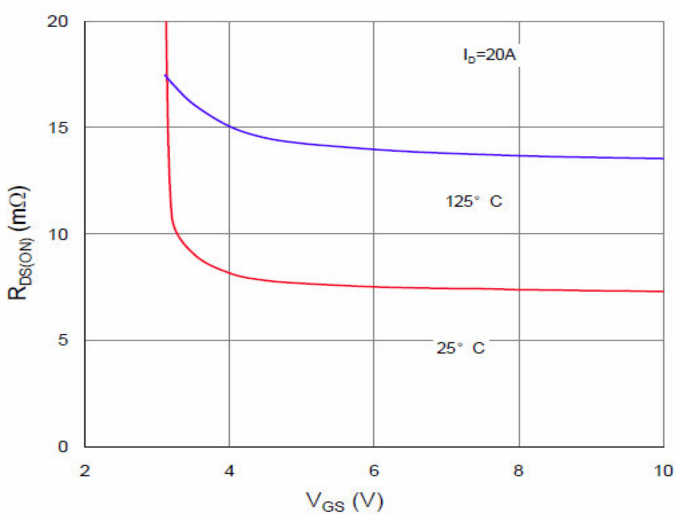


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

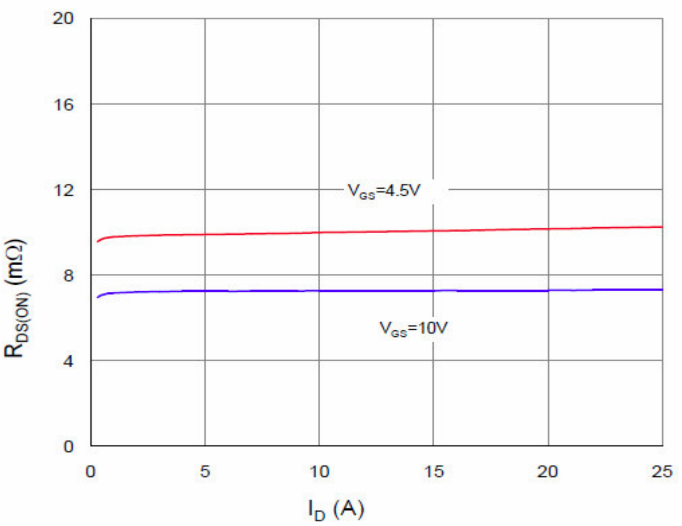


Figure 4. Normalized On-Resistance vs. Junction Temperature

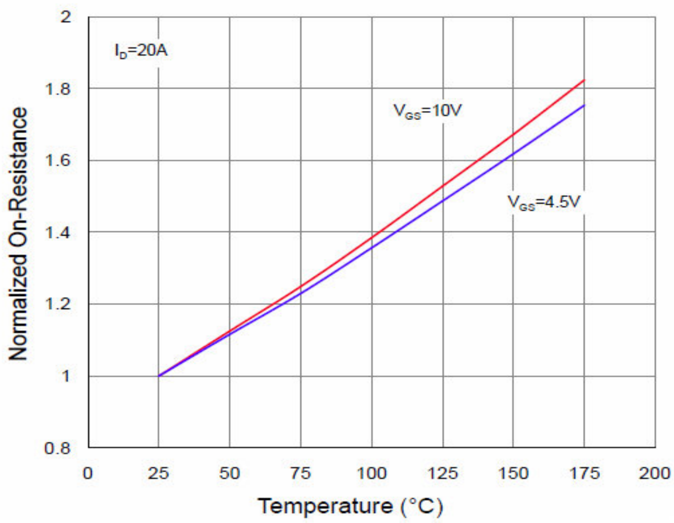


Figure 5. Typical Transfer Characteristics

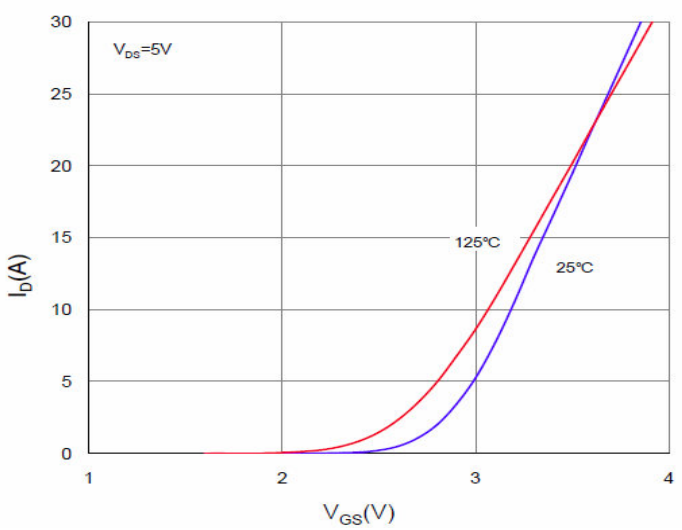
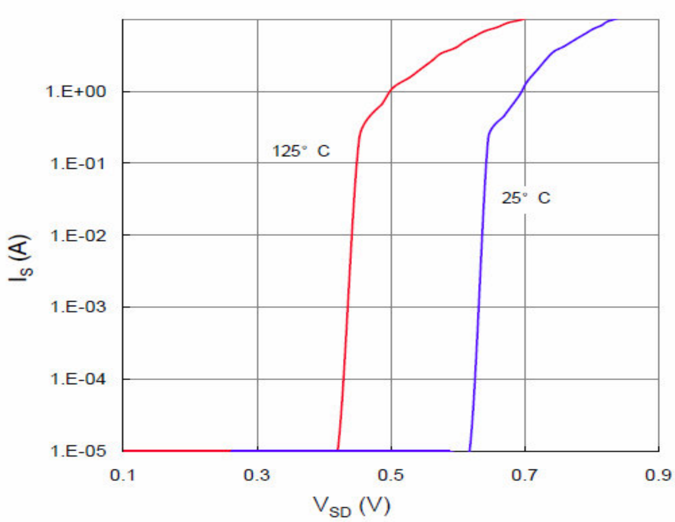


Figure 6. Typical Source-Drain Diode Forward Voltage



CHARACTERISTIC CURVES

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

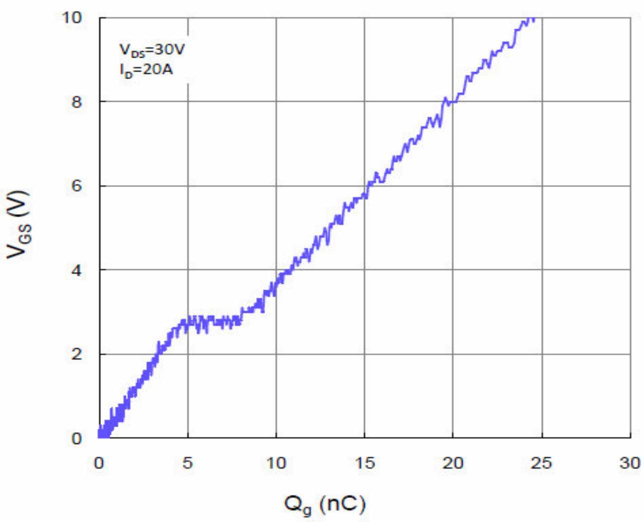


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

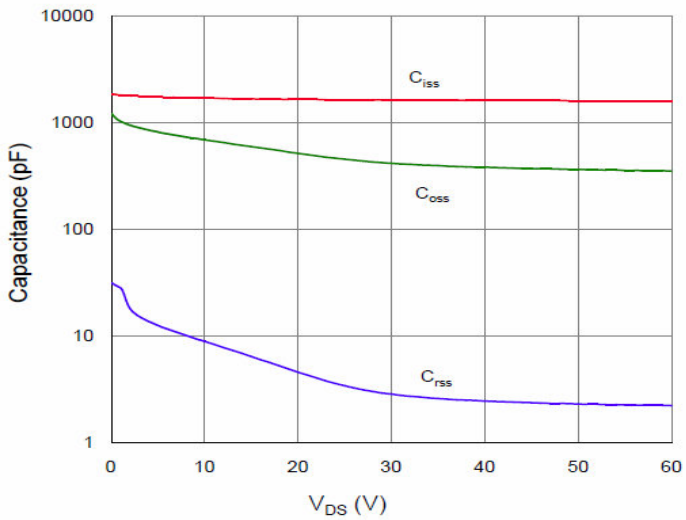


Figure 9. Maximum Safe Operating Area

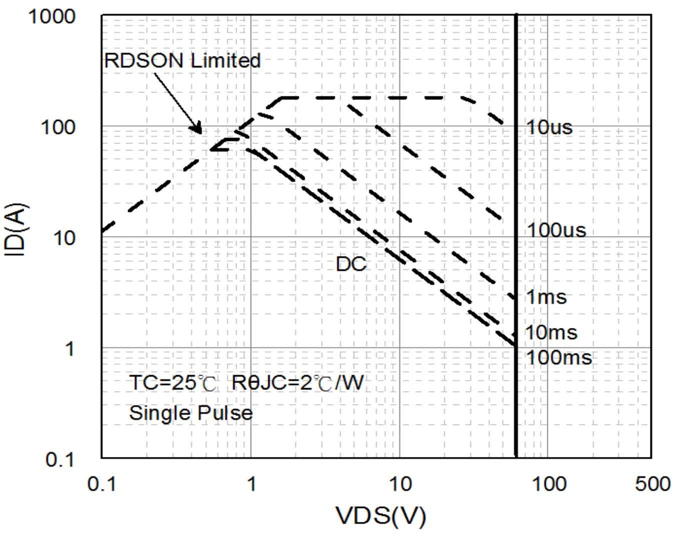


Figure 10. Drain Current vs. Case Temperature

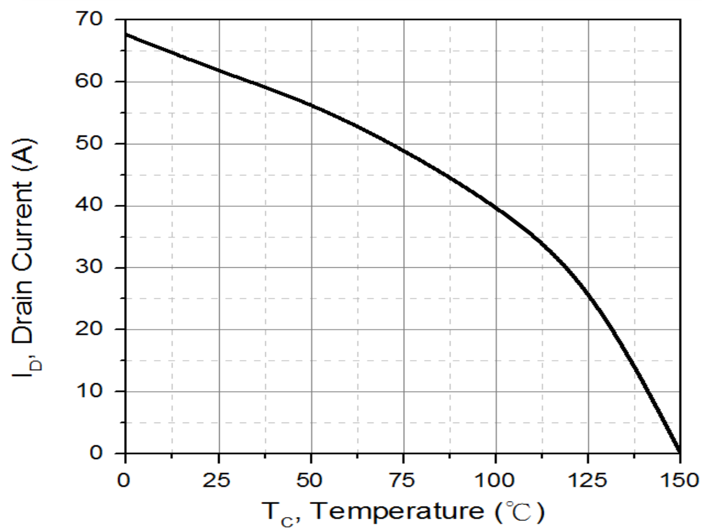


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case