Elektronische Bauelemente

# SSD75N06-C

**75A, 60V, $R_{DS(ON)}$ 8.5mΩ**

**N-Channel Enhancement Mode Power MOSFET**

RoHS Compliant Product

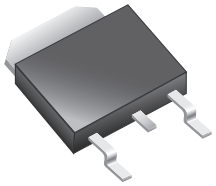
A suffix of "-C" specifies halogen & lead-free

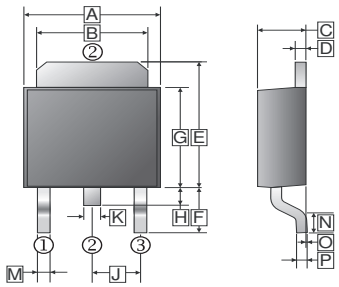
## DESCRIPTION

The SSD75N06-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The SSD75N06-C meet the RoHS and Green Product requirement with full function reliability approved.

**TO-252(D-Pack)**



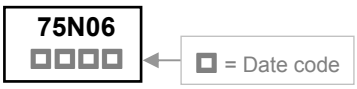



| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 6.30 | 6.90 | J | 2.30 REF. | |
| B | 4.95 | 5.53 | K | 0.89 REF. | |
| C | 2.10 | 2.50 | M | 0.45 | 1.14 |
| D | 0.40 | 0.90 | N | 1.55 TYP. | |
| E | 6.00 | 7.70 | O | 0 | 0.15 |
| F | 2.90 REF. | | P | 0.58 REF. | |
| G | 5.40 | 6.40 | | | |
| H | 0.60 | 1.20 | | | |

## FEATURES

- Lower Gate Charge
- Advanced high cell density Trench technology
- Green Device Available

## MARKING

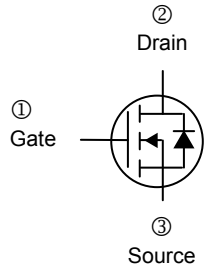



## PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---|---|---|
| TO-252 | 2.5K | 13 inch |

## ORDER INFORMATION

| Part Number | Type |
|---|---|
| SSD75N06-C | Lead (Pb)-free and Halogen-free |




## ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C unless otherwise specified)

| Parameter | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current [1] @$V_{GS}$=10V | $T_C$=25°C | $I_D$ | 75 | A |
| | $T_C$=100°C | | 47 | |
| Pulsed Drain Current [2] | | $I_{DM}$ | 200 | A |
| Power Dissipation | $T_C$=25°C | $P_D$ | 62.5 | W |
| Operating Junction & Storage Temperature | | $T_J$, $T_{STG}$ | -55~150 | °C |
| **Thermal Resistance Ratings** | | | | |
| Thermal Resistance Junction-Ambient [1] | | $R_{\theta JA}$ | 62 | °C/W |
| Thermal Resistance Junction-Case [1] | | $R_{\theta JC}$ | 2 | |

## ELECTRICAL CHARACTERISTICS ($T_J$=25°C unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 60 | - | - | V | $V_{GS}$=0, $I_D$=250μA |
| Gate-Threshold Voltage | $V_{GS(th)}$ | 1.2 | - | 2.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±20V |
| Drain-Source Leakage Current | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$=48V, $V_{GS}$=0, $T_J$=25°C |
| | | - | - | 5 | | $V_{DS}$=48V, $V_{GS}$=0, $T_J$=55°C |
| Static Drain-Source On-Resistance [3] | $R_{DS(ON)}$ | - | 6.5 | 8.5 | mΩ | $V_{GS}$=10V, $I_D$=10A |
| | | - | 8.8 | 12 | | $V_{GS}$=4.5V, $I_D$=5A |
| Gate Resistance | $R_g$ | - | 1.2 | - | Ω | $V_{DS}$=$V_{GS}$=0, f =1.0MHz |
| Total Gate Charge | $Q_g$ | - | 28 | - | nC | $I_D$=10A<br>$V_{DS}$=30V<br>$V_{GS}$=4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 8.6 | - | | |
| Gate-Drain Change | $Q_{gd}$ | - | 13.5 | - | | |
| Turn-on Delay Time [2] | $T_{d(on)}$ | - | 16.4 | - | nS | $V_{DD}$=30V<br>$I_D$=10A<br>$V_{GS}$=10V<br>$R_G$=3.3Ω |
| Rise Time | $T_r$ | - | 39.8 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 53.9 | - | | |
| Fall Time | $T_f$ | - | 15.2 | - | | |
| Input Capacitance | $C_{iss}$ | - | 3307 | - | pF | $V_{GS}$ =0<br>$V_{DS}$=30V<br>f =1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 201 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 151 | - | | |
| **Source-Drain Diode** | | | | | | |
| Diode Forward Voltage [3] | $V_{SD}$ | - | - | 1.2 | V | $I_S$=1A, $V_{GS}$=0 |
| Continuous Source Current [1] | $I_S$ | - | - | 75 | A | $V_G$=$V_D$=0, Force Current |
| Reverse Recovery Time | $T_{rr}$ | - | 19 | - | nS | $I_F$=10A, dI/dt=100A/μs<br>$T_J$=25°C |
| Reverse Recovery Charge | $Q_{rr}$ | - | 66 | - | nC | |

Notes:
1. The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width ≤300μs, Duty Cycle≤2%
3. The Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

## CHARACTERISTIC CURVES

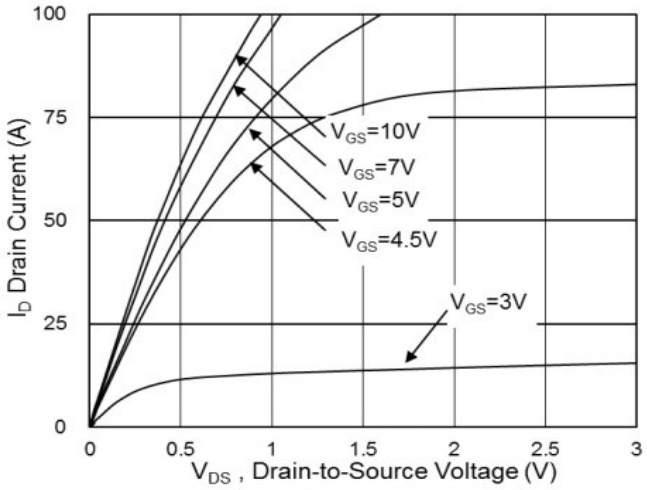



**Fig.1 Typical Output Characteristics**

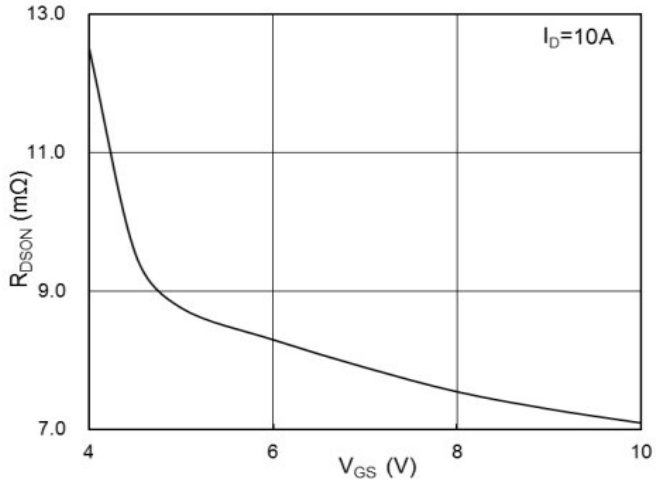



**Fig.2 On-Resistance vs Gate-Source Voltage**

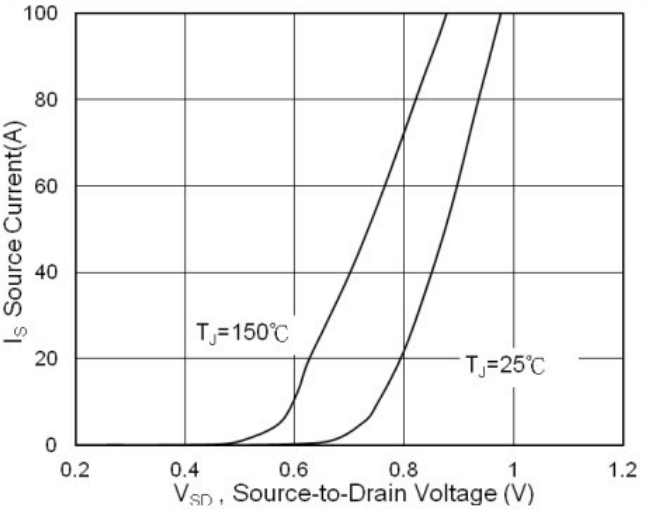



**Fig.3 Forward Characteristics of Reverse**

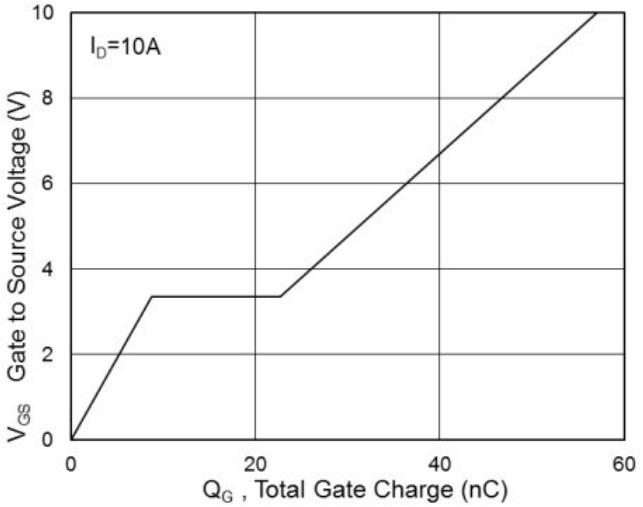



**Fig.4 Gate-Charge Characteristics**

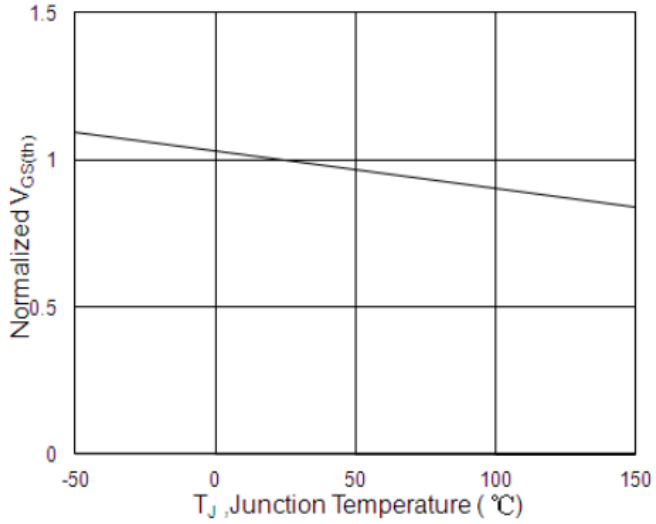



**Fig.5 Normalized $V_{GS(th)}$ vs $T_J$**

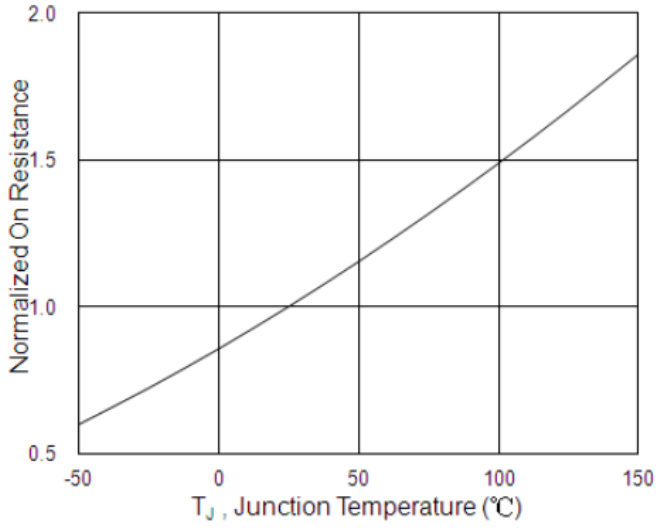



**Fig.6 Normalized $R_{DSON}$ vs $T_J$**

## CHARACTERISTIC CURVES

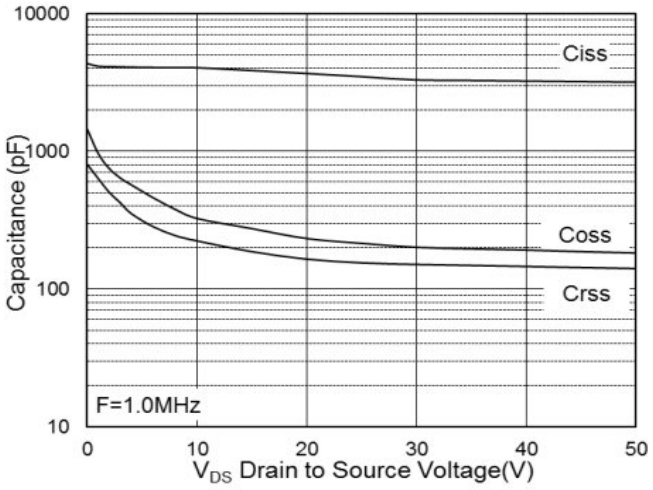



Fig.7 Capacitance

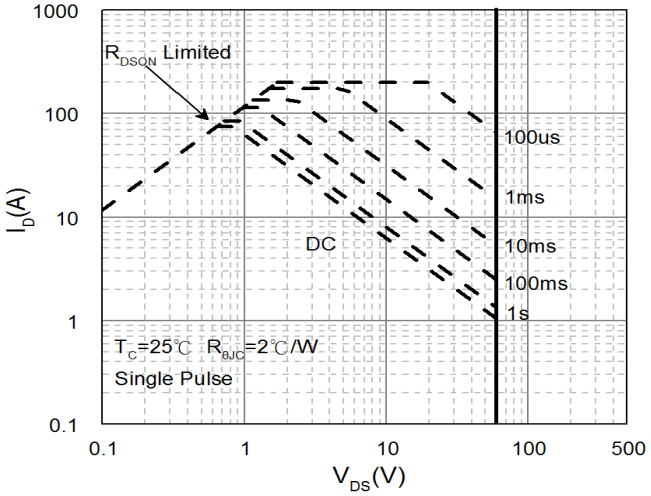



Fig.8 Safe Operating Area

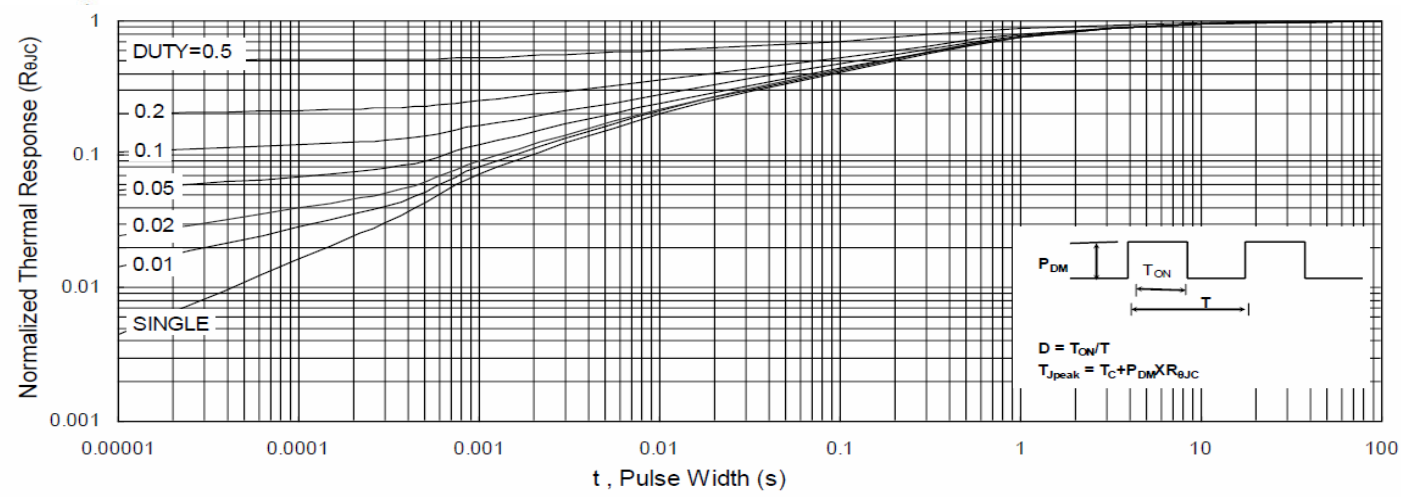



Fig.9 Normalized Maximum Transient Thermal Impedance

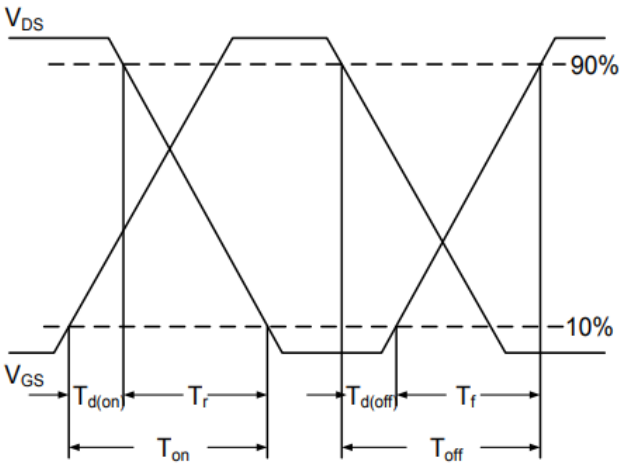



Fig.10 Switching Time Waveform

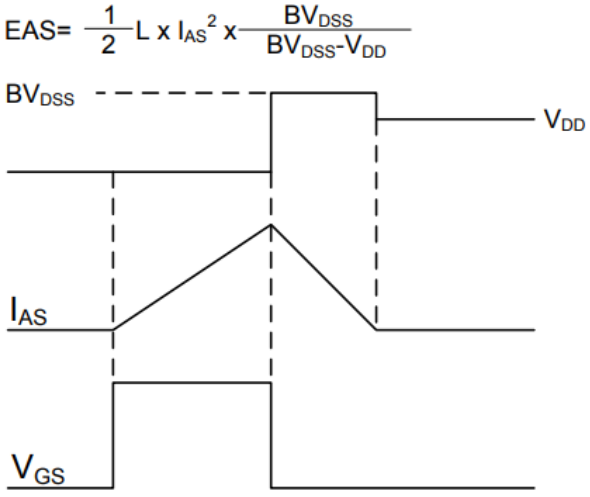



Fig.11 Unclamped Inductive Switching Waveform