

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

The SSU170N10SV-C is the highest performance N-Ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The SSU170N10SV-C meet the RoHS and Green Product requirement with full function reliability approved.

## FEATURES

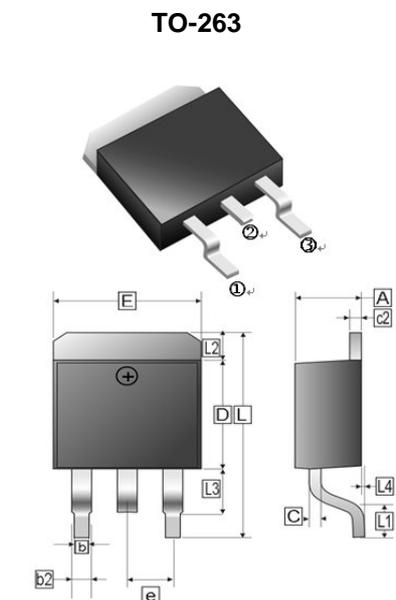
- High Speed Power Switching
- Super Low Gate Charge
- Green Device Available

## MARKING



## PACKAGE INFORMATION

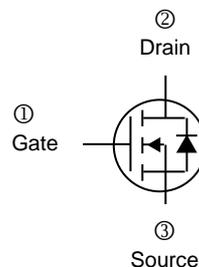
Package	MPQ	Leader Size
TO-263	0.8K	13 inch



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.00	4.87	c2	1.07	1.65
b	0.51	1.01	b2	1.34 REF.	
L4	0	0.30	D	8	9.65
C	0.30	0.74	e	2.54 REF.	
L3	1.50 REF.		L	14.60	16.10
L1	2.50 REF.		L2	1.27 REF.	
E	9.60	10.67			

## ORDER INFORMATION

Part Number	Type
SSU170N10SV-C	Lead (Pb)-free and Halogen-free



## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> @ $V_{GS}=10\text{V}$	$T_C=25^\circ\text{C}$	170	A
	$T_C=100^\circ\text{C}$	120	
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	380	A
Power Dissipation <sup>3</sup>	$P_D$	231	W
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55~175	$^\circ\text{C}$
<b>Thermal Resistance Rating</b>			
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	0.65	

**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Forward Transfer Conductance	$g_{fs}$	-	50	-	S	$V_{DS}=5V, I_D=20A$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V$
Drain-Source Leakage Current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$
		-	-	100		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	3.4	3.9	m $\Omega$	$V_{GS}=10V, I_D=20A$
Total Gate Charge	$Q_g$	-	75	-	nC	$I_D=20A$ $V_{DS}=50V$ $V_{GS}=10V$
Gate-Source Charge	$Q_{gs}$	-	10	-		
Gate-Drain Change	$Q_{gd}$	-	34	-		
Turn-on Delay Time	$T_{d(on)}$	-	13	-	nS	$V_{DD}=50V$ $I_D=20A$ $V_{GS}=10V$ $R_G=10\Omega$
Rise Time	$T_r$	-	19	-		
Turn-off Delay Time	$T_{d(off)}$	-	45	-		
Fall Time	$T_f$	-	27	-		
Input Capacitance	$C_{iss}$	-	3650	-	pF	$V_{GS}=0V$ $V_{DS}=50V$ $f=1\text{MHz}$
Output Capacitance	$C_{oss}$	-	1110	-		
Reverse Transfer Capacitance	$C_{rss}$	-	43	-		
<b>Source-Drain Diode</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1A, V_{GS}=0V$
Continuous Source Current <sup>1</sup>	$I_S$	-	-	170	A	$V_G=V_D=0, \text{Force Current}$
Reverse Recovery Time	$T_{rr}$	-	50	-	nS	$I_F=20A, dI/dt=500A/\mu s,$
Reverse Recovery Charge	$Q_{rr}$	-	275	-	nC	$T_J=25^\circ\text{C}$

Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed pulse width  $\leq 10\mu s$ , duty cycle  $\leq 2\%$ .
3. The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature.

**CHARACTERISTIC CURVES**

Fig 1. Typical Output Characteristics

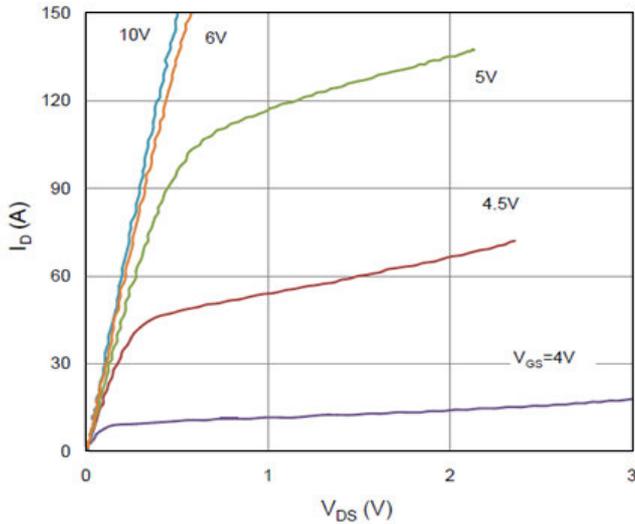


Figure 2. On-Resistance vs. Gate-Source Voltage

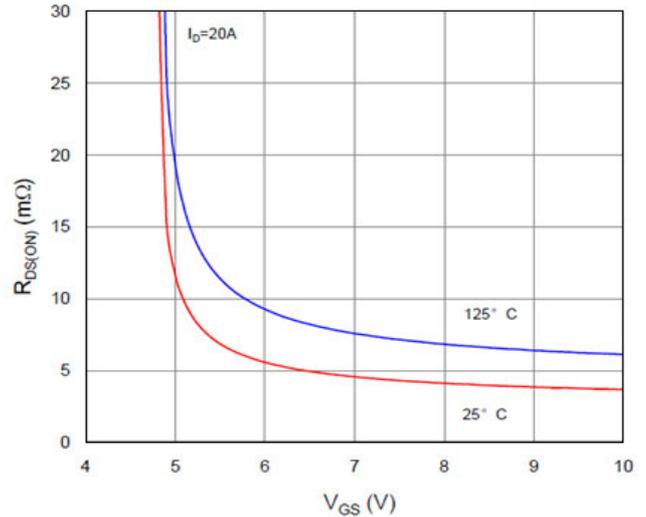


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

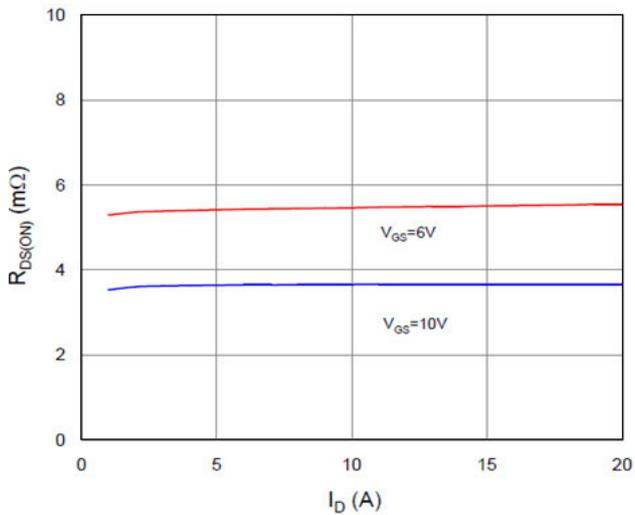


Figure 4. Normalized On-Resistance vs. Junction Temperature

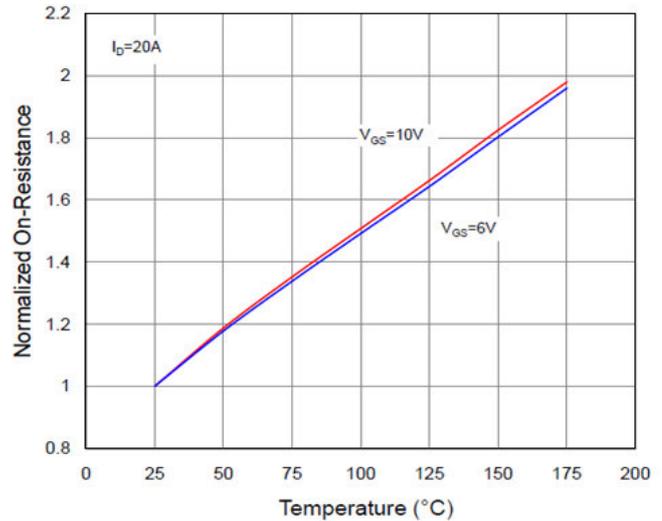


Figure 5. Typical Transfer Characteristics

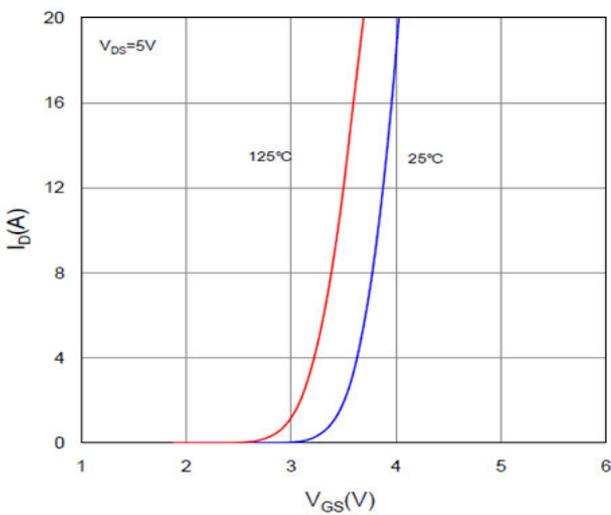
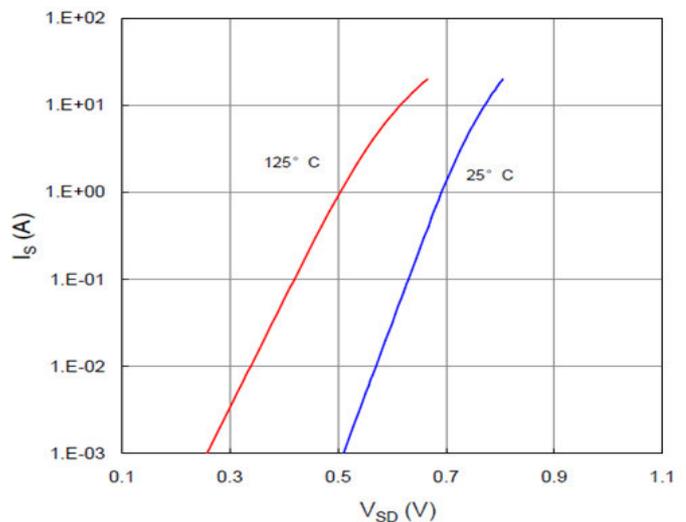


Figure 6. Typical Source-Drain Diode Forward Voltage



**CHARACTERISTIC CURVES**

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

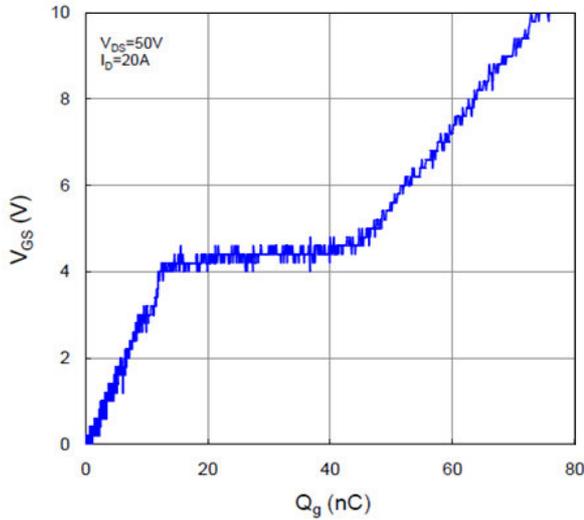


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

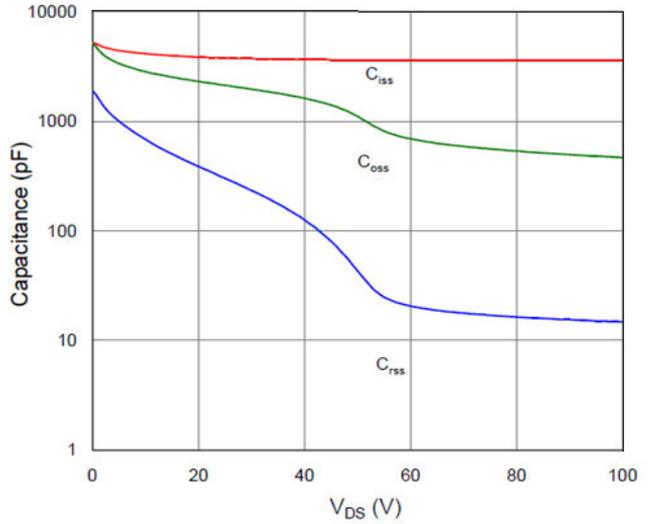


Figure 10. Maximum Drain Current vs. Case Temperature

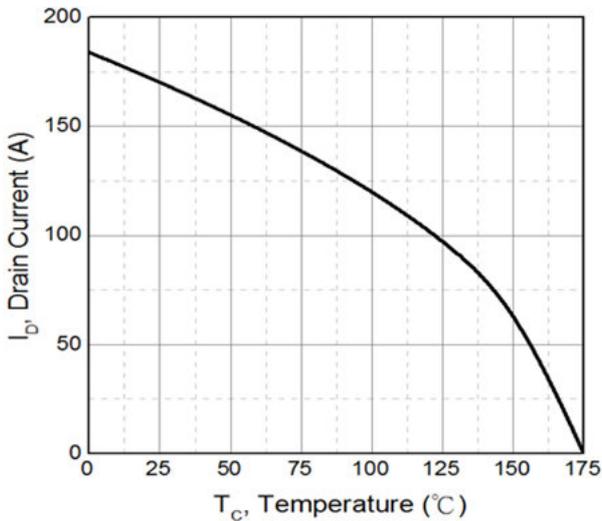


Figure 9. Maximum Safe Operating Area

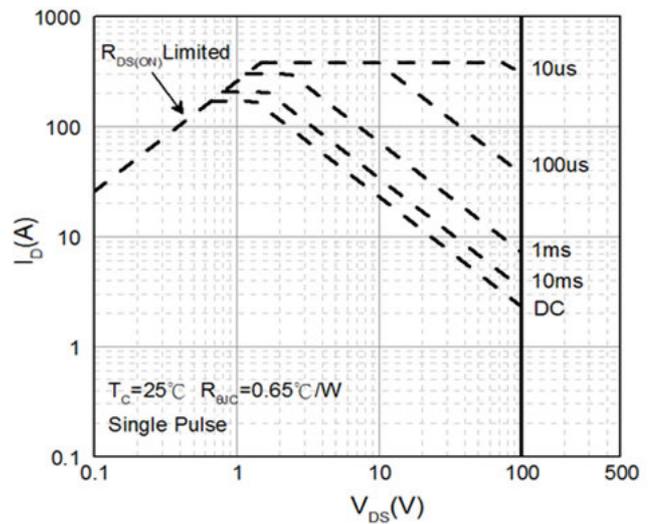


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

